AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (original) A production process for producing a plurality of semiconductor devices on chip areas which are defined on a wafer, which production process comprises:

processing said wafer such that each of said chip areas is produced as a semi-finished semiconductor device by forming a first wiring-arrangement section on each of said chip areas;

subjecting said wafer to a provisional yield-rate test in which it is examined whether each of the semi-finished semiconductor devices on said wafer is acceptable or unacceptable; and

further processing said wafer such that each of said chip areas is produced as a finished semiconductor device by forming a second wiring-arrangement section on said first wiring-arrangement section when said wafer passes said provisional yield-rate test.

2. (original) A production process as set forth in claim 1, wherein a yield-rate of acceptable semi-finished semiconductor devices is found in said provisional yield-rate test, and it is determined that said wafer has passed said

provision yield-rate test when said yield-rate exceeds a predetermined permissible rate.

3. (original) A production process as set forth in claim 1, wherein said first wiring-arrangement section is formed as a basic wiring-arrangement section to define plural kinds of basic electronic component formation areas in each of said chip areas, and said second wiring-arrangement section is formed as a customized wiring-arrangement section to establish electrical interconnections among said basic electrical component formation areas in accordance with a customer's request.

4. (original) A production process as set forth in claim 1, wherein said basic wiring-arrangement section has a plurality of electrode pads formed on an uppermost surface thereof, for carrying out said provisional yield-rate test.

5. (original) A production process as set forth in claim 1, further comprising:

subjecting said wafer to a genuine yield-rate test in which it is examined whether each of the finished semiconductor devices on said wafer is acceptable or unacceptable to thereby find a yield-rate of acceptable finished semiconductor devices; and

finally processing said wafer when said wafer passes said genuine yield-rate test.

6. (original) A production process as set forth in claim 5, wherein a yield-rate of acceptable finished semiconductor devices is found in said genuine yield-rate test, and it is determined that said wafer has passed said genuine yield-rate test when said yield-rate exceeds a predetermined permissible rate.

7. (original) A production process as set forth in claim 5, wherein said customized wiring-arrangement section has a plurality of electrode pads formed on an uppermost surface thereof, and said genuine yield-rate test is carried out, using the electrode pads of said customized wiring-arrangement section.

8. (original) A production process as set forth in claim 7, wherein said basic wiring-arrangement section is formed as a multi-layered wiring-arrangement section composed of at least two metal circuit pattern layers and at least one insulation layer alternately laminated on each of said chip areas, and said customized wiring-arrangement section is formed as a multi-layered wiring-arrangement section composed of at least two metal circuit pattern layers and at least one insulation layer alternately laminated on said basic wiring-arrangement section.

9-23. (canceled)